Abstract of Disclosure

A smart memory comprising SIMD processing elements is disclosed. Each SIMD processing element contains individually addressable registers that give the smart memory the functionality of random access memory. An activation rule activates all the SIMD processing elements whose element addresses are (1) no less than a start address; (2) no more than an end address, and (3) an increment of a carry number starting from the start address, in which the carry number could be a constant of one in the constructs for some application. Neighboring SIMD processing elements can be connected to allow local operations involving neighboring the SIMD processing elements. This memory carries out parallel processing on data within itself of those simple parallel operations that are universal to all elements, or only involve neighboring memory elements. For an array of N items, this smart memory reduces the total instruction cycle count of universal operations such as insertion and match finding to ~ 1, local operations, such as filtering and template matching, to ~ local operation size, and global operations such as sum and limit finding to ~ sqrt(N). Particularly, this smart memory eliminates most data transportation activities for data processing purpose on the system bus. Yet this smart memory is easy to use, pin and functional compatible with conventional random accessible memory, and practical for implementation.